UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/843,178	04/26/2001	Jason Gosior	116.003	9171

31209 7590 01/29/2007

DONALD V. TOMKINS
C/O TOMKINS LAW OFFICE
740, 10150 - 100 STREET
EDMONTON, AB T5J 0P6
CANADA

EXAMINER	
LI, AIMEE J	
ART UNIT	PAPER NUMBER
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/843,178	GOSIOR ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been considered. Claim 1 has amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 05 November 2006; RCE as filed 05 November 2006; Rule 130, 131 or 132 Affidavit as filed 05 November 2006; and Extension of Time for Three Months as filed 05 November 2006.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05 November 2006 has been entered.

Examiner Notes

4. The Examiner notes that the application history indicates that page 291 of Steve Furber's Arm System-on-Chip Architecture ©2000 was not provided to Applicant, even though it was cited in the Final Rejection dated 04 May 2006. The Examiner assumes that, since no questions or arguments were made towards the missing page, the Applicant had a copy of the page. The Examiner has included this page with the current action to clarify the record, but has not changed the rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM).

7. Regarding claim 1, Li has taught a programmable, single-chip embedded processor, comprising:

a. A multiple-bit, multithread processor core comprising a single processor pipeline having 'k' pipeline stages shared by one or more independent processor threads, the number 'k' being equal to at least four, and the number 'n' of said processor threads being equal to or less than 'k' (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, the multiple pipelines taught is due to the multiple functional units with individual execution pipelines, which have various numbers of stages (Li Section 1 Introduction, paragraphs 1-2 and Section 2 A FPMP Architecture, paragraph 1). Li further states in Section 1 Introduction, paragraph 7, that when

the number of threads is equal to number of stages in a pipeline, the utilization of the pipeline is 100%, thereby taking full advantage of the benefits to pipelining.

b. An instruction execution logic mechanism engaged with said processor core for executing instructions from a built-in instruction set (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, Figure 1 shows multiple execution units used to execute instructions in the system.

c. A supervisory control unit, controlled by one or more control threads selected from said processor threads, for examining the processor core state and for controlling the operation of said processor core (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, Section 2 A FPMP Architecture describes Figure 1, including the Thread Dispatch Unit and Instruction Scheduling Unit, which select and schedule instructions from the different threads for execution based upon a round robin scheduling strategy and scoreboard mechanism that checks for source operand availability.

d. A memory capable of storing data comprising instructions from said instruction set (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A

FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, Section 2 A FPMP Architecture, paragraph 2 states that there is an instruction cache for each thread slot to store a threads instructions.

e. Wherein:

i. Each or the 'n' program threads occupies a unique pipeline stage at any given time (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, a pipeline operates, ideally, by dispatching one instruction each cycle. This means that an instruction iterates through a pipeline, e.g. occupies separate successive stages, each cycle until it is output for storage into the registers.

ii. Each program thread advances to the next pipeline stage with every clock cycle (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, a pipeline operates, ideally, by dispatching one instruction each cycle. This means that an instruction iterates through a pipeline, e.g.

occupies separate successive stages, each cycle until it is output for storage into the registers.

iii. For a given program thread, the pipeline completes a one-word instruction every 'k' clock cycles (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, a pipeline operates, ideally, by dispatching one instruction each cycle. This means that an instruction iterates through a pipeline, e.g. occupies separate successive stages, each cycle until it is output for storage into the registers at the end of the pipeline. Hence, the time it takes to complete an instruction is equal to the number of pipeline stages times the number of clock cycles per stage, which is one clock cycle in Li.

8. Li has not taught

a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation;

b. Said memory being internally integral to the processor, and comprising a main RAM and a boot ROM; and

c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core.

9. ARM has taught

a. Said supervisory control unit being adapted to allow the one or more control threads to set up the initial state of one or more other threads and to start and stop their operation (ARM page 291). In regards to ARM, an operating system is essentially a control thread, since it determines indicates when a thread is to start and stop running (ARM page 291, paragraph 3-4).

b. Said memory being internally integral to the processor (ARM page 271), and comprising a main RAM and a boot ROM (ARM pages 20 and 271). In regards to ARM, states on page 20, paragraph 4 and page 271 that on-chip RAM and microcode ROM are both commonly used types of memory.

c. A peripheral adaptor internally integral to the processor and engaged with said processor core for transmitting input/output signals to and from said processor core (ARM pages 216-217). In regards to ARM, Figure 8.11 is for an advanced on-chip bus architecture connecting various elements of the chip, which includes a peripheral bus connecting on-chip peripheral interfaces to the rest of the chip, including the core.

10. A person of ordinary skill in the art at the time the invention was made, and as taught by ARM, would have recognized that the details of an embedded system such as ARM reduces power consumption by minimizing off-chip activity, e.g. fewer loads from off-chip memory, and

increases parallelism (ARM pages 31-32). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the embedded details of ARM in the device of Li to reduce power consumption.

11. Regarding claim 3, Li has taught a system as recited in claim 1, wherein said processor core supports "n" multiple groups of independent threads by replicating said common execution logic and said memory (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). In regards to Li, Figure 1 shows multiple execution units used by all threads, e.g. common execution units, and states in Section 2 A FPMP Architecture that there are separate instruction caches for each thread slot.

12. Claims 2, 6-7, 9-10, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady).

13. Li has taught wherein said memory comprises internal memory for storing and executing core processor code (Li Abstract; Section 1 Introduction, paragraphs 2, 5, and 8; Section 2 A FPMP Architecture, paragraphs 1, 4, and 6; Section 3 The Analytic Model, paragraph 5; Section 4 Examples and validation, paragraph 8; Section 5 Conclusion, paragraph 1; Figure 1; Figure 2; and Figure 3). Li has not taught

a. (Claim 2) A system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage, instruction decode logic stage, multiple port register read stage, address mode logic stage, arithmetic logic unit for arithmetic and address calculations stage, multiple port memory stage, branch/wait logic stage, and multiple port register write stage;

b. (Claim 6) A system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity;

c. (Claim 7) A system as recited in claim 1, wherein said supervisory control unit is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation;

d. (Claim 9) A system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions;

e. (Claim 10) A system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads;

f. (Claim 16) A system as recited in claim 1, wherein said memory comprises external memory engaged with said peripheral adaptor; and

g. (Claim 17) A system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.

14. Parady has taught

a. (Claim 2) A system as recited in claim 1, wherein said processor pipeline includes an instruction fetch logic stage (Parady Col.3 lines 2-9), instruction decode logic stage (Parady 14 of Fig.3), multiple port register read stage (Parady 48/50 of Fig.3), address mode logic stage (Parady Col.3 lines 2-9), arithmetic logic unit for arithmetic and address calculations stage (Parady Col.3 lines 50-56), multiple port memory stage (Parady 48/50 of Fig.3), branch/wait logic stage (Parady 18 of Fig. 1), and multiple port register write stage (Parady 48/50 ofFig.3). Here, the functions are not shown to be explicit stages of operation in the pipeline, but being that the UltraSparc processor of Parady (see Col.2 lines 66-67) is pipelined (see Col.3 lines 35-43), it is inherent that the operations of these units occur in a pipelined fashion.

b. (Claim 6) A system as recited in claim 1, wherein said instruction set includes a processor instruction for enabling individual threads to determine their thread identity (Parady Fig.4 and Col.3 line 66 - Col.4line 8). Here, certain instructions can enable a specific thread upon a thread switch, thus determining the identity of the thread that is desired to be switched to.

c. (Claim 7) A system as recited in claim 1, wherein said supervisory control unit (Parady 112 of Fig.3) is capable of examining and interpreting the state of multithread processor core operation for the purpose of starting, stopping, and modifying individual multithread processor operation (Parady Col.3 lines 57-65). Here, the thread switching logic monitors the processing core for a cache miss, and if it determines there was a cache miss, can stop the current thread and start a

new thread (Parady Col.3 lines 57-65), as well as put the threads into interleaving mode (Parady Col.4 lines 18-29).

d. (Claim 9) A system as recited in claim 1, wherein said supervisory control unit is capable of being accessed and controlled by each of said operating core processor threads by using input/output instructions (Parady Col.3 line 57 - Col.4 line 8). Here, each thread can access the thread switching logic by providing it with a thread ID to switch to upon a long-latency operation which is detected by the thread switching logic, the thread ID which can be provided in a load or store (input/output) instruction (see Col 4 lines 5-7).

e. (Claim 10) A system as recited in claim 9, wherein said controlling operating processor thread is programmable and comprises any of the available threads (Parady Col.3 line 57 – Col 4 line 8). Here, any of the four threads can cause a cache miss to be detected by the thread switching logic (Parady Col.3 lines 57-65), and can further be programmed to include a thread field that tells the thread switching logic which thread to switch to (Parady Col 4 lines 1-8).

f. (Claim 16) A system as recited in claim 1, wherein said memory comprises external memory engaged with said peripheral adaptor (Parady 176/180 of Fig.5).

g. (Claim 17) A system as recited in claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core (Parady Fig.3). Here, the thread switching logic is separate from the core functions of fetch, decode, issue and execute.

15. A person of ordinary skill in the art at the time the invention was made, and as taught by Parady, would have recognized that the device of Parady improves thread switching efficiency (Parady Col. 2 lines 15-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the device of Parady in the device of Li in view of ARM to improve thread switching efficiency.

16. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Dickman et al., U.S. Patent No. 4,556,951 (herein referred to as Dickman).

17. Regarding claim 4, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught wherein the system further comprises a condition code mechanism implemented in said instruction set for detecting specific word data types. However, Dickman has taught a system for detecting specific word data type and setting corresponding condition codes so that conventional program control instructions can be used to control processing, rather than modifying existing control instructions to do so (Dickman Col.2 line 57 - Col.3 line 5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to detect specific types of data words and set their corresponding condition codes so that existing control instructions can be used, thereby creating less work and preserving the previous compatibility of the instruction set.

18. Regarding claim 5, Li in view of ARM and in further view of Dickman has taught a system as recited in claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range (Dickman Co1.8 line 63 - Col.9 line 12).

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady), as applied to claim 7 above, and further in view of Miyamoto et al., U.S. Patent No. 6,101,569 (herein referred to as Miyamoto).

20. Regarding claim 8, Li in view of ARM and in further view of Parady has taught a system of claim 7, but has not explicitly taught wherein the system further comprises a hardware semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral and system memory. However, Miyamoto has taught a semaphore vector (Miyamoto Cots lines 34-51) which controls multithread access to peripherals and system memory (Miyamoto Col.4 line 66 - Col.5 line 33) so that data is not inadvertently destroyed by another thread (see Col.1 lines 21-36). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to include the use of hardware semaphore vector to control access to peripherals and memory so that inadvertent data destruction does not take place, and thus incorrect operation does not result.

21. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE

©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and in further view of Parady, U.S. Patent No. 5,933,627 (herein referred to as Parady), as applied to claim 9 above, and further in view of Fernando et al., U.S. Patent No. 6,272,616 (herein referred to as Fernando).

22. Regarding claim 11, Li in view of ARM and in further view of Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating core processor thread is capable of reconfiguring the overall thread processing method of operation so that other processing threads can support multiple instruction multiple data processing operations. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Col.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (Fernando Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for an instruction that lets the processing threads switch into MIMD mode in order to improve processing performance for a broad range of software types.

23. Regarding claim 12, Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread can reconfigure the overall thread processing method of operation so that other processing threads can support single instruction multiple data processing operations. However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Col.2 lines 58-63) so that processing perfol111ance can be increased for a

broad range of software types and requirements (Fernando Col.2 lines 27-32). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for an instruction that lets the processing threads switch into SIMD mode in order to improve processing performance for a broad range of software types.

24. Regarding claim 13, Li in view of ARM and in further view of Parady has taught the system as recited in claim 9 above, but has not explicitly taught wherein said controlling operating processor thread is capable of reconfiguring the overall thread processing method of operation so that an arbitrary number of processing threads can support simultaneously single instruction multiple data processing operations and multiple instruction multiple data processing operations. However, However, Fernando has taught an instruction that allows current processing threads of execution to switch into a SIMD mode or a MIMD mode (Fernando Co1.2 lines 58-63) so that processing performance can be increased for a broad range of software types and requirements (Fernando Col.2 lines 27-32), which allows SIMD and MIMD modes to be concurrently executing (Fernando Col.l2 lines 1-5). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM and in further view of Parady to allow for the processing threads to simultaneously execute in both SIMD mode and MIMD mode in order to improve processing performance for a broad range of software types.

25. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture

Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Bishop et al., U.S. Patent No.5, 784,552 (herein referred to as Bishop).

26. Regarding claim 14, Li in view of ARM has taught the system as recited in claim 1, but has not explicitly taught wherein said supervisory control unit is operable by a first thread process to start and stop another thread process and to examine and alter state information in single step and multiple step modes of controlled operation. However, Bishop has taught the execution of an application program under the supervision of a debugging program, the debugging program which halts the application program (Bishop Col.5 lines 11-22) and can examine and alter state information via debugging instruction execution in either single-step or multi-step modes of debugging (Bishop Col.7 lines 13-45) so that an application programmer can more thoroughly test and debug their programs in a controlled testing environment (Bishop Col.1 lines 17-35). One of ordinary skill in the art would have recognized that thoroughly tested and debugged programs are less likely to fail and' provide incorrect results. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to allow a debugging program to stop and start another program so that instructions in the other program can be thoroughly tested and debugged in both single-step and multi-step modes of debugging.

27. Claims 15 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1

above, and further in view of Zammit et al., European Patent Application No. 1091292 (herein referred to as Zammit).

28. Regarding claims 15 and 19-20, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught

a. Wherein the system further comprises identifying bit patterns embedded in the unassigned bit fields of the machine instructions of said core processor (Applicant's claim 15);

b. Wherein said identifying bit pattern is used to identify programming code for code protection purposes (Applicant's claim 19); and

c. Wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism (Applicant's claim 20).

29. However, Zammit has taught a processor which identifies values in unused bit fields of instruction during a conversion so that the unused bit fields which contain inappropriate values, which could result in incorrect translation, can be corrected before being executed (see p3 lines 9-16, 35-39). This bit pattern also protects programming code from being incorrectly translated and causing incorrect execution of the program code. This bit pattern also does not affect the instruction execution logic operation, since it is only used to identify whether there are unused bit fields, which contain in appropriate values, and does not cause the execution logic to perform differently from what the instruction intended. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of Arm to identify values of unused bits so that inappropriate values are not incorrectly translated, and thus incorrect execution does not occur.

30. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" IEEE ©1995 (herein referred to as Li) in view of Steve Furber's ARM System-on-Chip Architecture Second Edition © 2000 (herein referred to as ARM), as applied to claim 1 above, and further in view of Wilske, U.S. Patent No. 4,155,115 (herein referred to as Wilske).

31. Regarding claim 18, Li in view of ARM has taught a system as recited in claim 1, but has not explicitly taught wherein said peripheral adaptor is capable of controlling analog and digital processing functions. However, Wilske has taught a microprocessor system which has a peripheral controller capable of receiving and controlling inputs from both analog and digital sources (Wilske Col.2 lines 7-34) so that both types of sources can be controlled from one location in order to reduce cost and lessen hardware (Wilske Col.1lines 14-24). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Li in view of ARM to allow its peripheral adapter to control both analog and digital sources so that the amount of hardware needed to control both types of sources can be reduced, thus lowering cost.

Response to Arguments

32. Applicant's arguments filed 05 November 2006 have been fully considered but they are not persuasive. Applicant's arguments are based upon the validity and sufficiency of the Declaration under 37 C.F.R. §1.132 from Mr. Jason J. Gosior filed on 05 November 2006. The Declaration under 37 CFR 1.132 filed 05 November 2006 is insufficient to overcome the rejection of claims 1-20 based upon Li in view of Arm and in further view of Parady, Dickman, Bishop, Zammit, Wilske, Miyamoto, and/or Fernando as set forth in the last Office action, and reiterated above, because:

a. Paragraphs 1-3 of the Declaration establish Mr. Gosior's expertise in the area Computer Architecture, his relationship to the Assignee, and his specific role with regards to the instant application. Since the Declaration is attempting to establish Commercial Success to overcome the current combination rejection, Mr. Gosior's expert opinion was relied upon to establish the presence of Commercial Success and its relationship to the claimed invention. However, Mr. Gosior is also a co-inventor of the instant application, and, while he is an expert in the field, he has a greater interest in the instant application's patentability. Consequently, Mr. Gosior's standing with regards to the instant application needs to be taken into consideration when analyzing the opinion he put forth in the Declaration.

b. Paragraph 4 of the Declaration establishes the nature of the Declaration, which is to establish evidence of commercial success for the claimed invention.

c. Paragraph 5 of the Declaration establishes that the claimed multithreaded architecture of Claim 1 was used by EEI to create RF communication solutions. Specifically, the paragraph establishes that the "XInC"™ and "XInC2"™ microcontrollers are the claimed invention. However, Mr. Gosior has not provided factual evidence to this fact. Mr. Gosior has provided no external evidence, such as overview documentation showing the "XInC"™ and "XInC2"™ architecture, showing the chips nor has he provided an explanation of how each of the limitations in Claim 1 relate to a specific element in the microcontroller architecture.

d. Paragraph 6 of the Declaration establishes the number of microcontrollers shipped and in production. However, Mr. Gosior has not provided factual evidence to this fact. The numbers are assertions by Mr. Gosior that these are the number of microcontrollers sold and the number being produced. Also, Mr. Gosior has not provided any type of comparison, supported by factual evidence, between these sales and production numbers and a competitor's sales and production numbers to show that these chips are a commercial success in its market.

e. Paragraph 7 of the Declaration establishes the customer base buying the microcontroller and how the customers used the microcontroller. However, there is no factual evidence, such as product documentation about the customers' products stating they use the microcontrollers produced by EEI in the products, support these assertions.

f. Paragraphs 8-11 of the Declaration establish what product the customers actually bought, i.e. the microcontroller with EEI's "Squeak"™ DWA system, and the reasons for the customers buying this product. Again, Mr. Gosior has provided no factual evidence for his assertions on the customers' reasoning. The statements supported Mr. Gosior's assertions or results of the customers' comparative tests were not provided. Also, the customers tested the DWA system as a whole, not the specific claimed invention, and the results, therefore their reasons for purchasing the microcontroller, were based upon the entire DWA system, not just the microcontroller. As Mr. Gosior states in paragraph 8, "The XInC microcontroller is...the primary component of the 'Squeak' system." This

implies that the microcontroller claimed is not the sole element in the DWA system, so, without further factual evidence, there is no evidence displaying that the DWA system was purchased because of the microcontroller not some other element in the DWA system. In addition, the paragraphs describe how the DWA system provides a better QoS than competitors' systems without factual evidence. The Examiner is unsure whether Mr. Gosior is attempting to establish commercial success at this point in the Declaration or unexpected results. In either case, factual, extrinsic evidence showing the differences between the DWA system and competitors' systems must be provided to support Mr. Gosior's assertion.

g. Paragraphs 12-14 of the Declaration establish the connection between the DWA system and the microcontroller and the advantage to using the DWA system. However, there is no factual evidence supporting Mr. Gosior's assertion and there is no clear nexus between the broadly claimed embedded processor of Claim 1 and the XInC microcontroller. The technical discussion in paragraphs 13-14 describes the DWA system with Appendix A assisting in illustrating Mr. Gosior's discussion about the technical merits of the pipeline. However, the discussion is about the specific DWA system and its performance when in a multi-threaded, pipelined system. The Examiner recognizes that this could potentially be linked to limitations (f)-(h) in Claim 1 but not to limitations (a)-(e), and there is no clear discussion of the nexus between limitations (f)-(h) in Claim 1 to the pipeline in Appendix A. Also, the evidence must be "commensurate in scope with the claims, the commercial success must be due to claimed features, and not due to

unclaimed features (MPEP 716.03(a))." The current claims recite a general multi-threaded, pipelined embedded processor. The pipelines in Appendix A functions as it does and produces the results discussed in paragraph 13 partly because of the claimed pipeline but also because of the specific separation of threads Mr. Gosior describes in paragraph 14. According to paragraph 14, the pipeline could not achieve such latency results without the processing time being balanced across the threads, which is not part of the claim. Therefore, assuming the commercial success of the DWA system is due to the better performance and not other extrinsic factors, such as advertising, business events, or consumption by regular customers, the commercial success of the DWA system is not directly derived from the claimed feature (MPEP 716.03(b)). For example, *In re Tiffin* 448 F.2d 791, 171 USPQ 294(CCPA 1971) had evidence showing commercial success of thermoplastic foam "cups" used in vending machines, but that was not commensurate in scope with the claims of thermoplastic foam "containers" in general, which is similar to the current situation. The DWA system in the Declaration is a specific implementation and use of the embedded processor in Claim 1, but this specific system is much narrower in scope than the broadly claimed processor. The processor in Claim 1 does not necessarily have to be used in the DWA system, so it would not necessarily be implementing the Squeak protocol in paragraph 12 and executing the threads described in paragraph 14. Consequently, the achievements that Mr. Gosior states are the very reason why customers buy the DWA system would not be achieved, so the embedded

processor claimed would not be bought. Claim 1's language, with regards to the multi-threaded pipeline, merely states that the embedded processor is a finely concurrent multithreaded processor (FCMP), also called a simultaneous multithreaded processor (SMP), which have separate, independent threads executing in the pipeline at the same time. In order to achieve this, FCMP or SMP have independent thread with an instruction in a separate pipeline stage, which are moved through each stage in the pipeline. There is no language in the claims reflecting the Squeak protocol and thread division that are necessary to achieve the results that Mr. Gosior asserts are the reasons for the commercial success. It is the Examiner's opinion that the Declaration provides a commercial success argument for the DWA system as a whole not just the embedded processor claimed.

h. Paragraphs 15-16 of the Declaration establish the differences between the DWA system and the prior art, particularly the sequential pipeline of Parady. The Examiner agrees that there are distinct differences between a multi-threaded sequential pipeline and the DWA system pipeline, but the Final Rejection dated 04 May 2006 relied upon Li et al.'s "The Effect of STEF in Finely Parallel Multithreaded Processors" ©1995, which is not a multi-threaded sequential pipelined processor, referred to as "Coarsely Concurrent Multithreaded Processor (CCMP)" in Li, but an FPMP that executes multi-threads in a pipeline simultaneously in view of Steve Furber's ARM System-on-Chip Architecture ©2000, which is an analysis of the commercially available ARM embedded

processors' architectures. The DWA system, as described by Mr. Gosior, appears to use an FPMP type multi-threaded pipeline, since it has multiple instructions from separate independent threads executing simultaneously in the pipeline. Parady was used to reject dependent claims reciting details of a pipelined multi-threaded processor that Li did not teach and are well-known in the art to be needed in any type of multi-threaded pipelined processor. To argue the differences between the current claimed invention, the focus should be on Li, which is the Examiner believes is, to date, the closest piece of art cited to Applicant. The Examiner recognized the differences between a multi-threaded sequential pipeline, such as that in Parady, and the claimed invention. Hence, Li, not Parady, was used as the primary reference in the combination rejection. The Examiner did locate a typographical error in the Final Rejection dated 04 May 2006 in paragraph 3. The Examiner stated "Regarding claim 3, Parady has taught..." but the citation following the claim was from Li. The language should have been "Regarding claim 3, Li has taught..." to match the citation. The typographical error has been corrected above.

i. Paragraph 17 concludes the Declaration and summarizes the Declaration by stating that the results behind the customers' reasons for purchasing the DWA system were a direct result of the claimed processor architecture. However, throughout the entire Declaration there was no clear nexus between the claim language and features found in EEI's XInC processor nor was there evidence of a nexus between the claim language and the XInC processor. Also, there was no

factual evidence provided to support the Declarations assertion of commercial success, such as sales figures from EEI and competitors; the performance achievements are a direct result of the claimed architecture not the entire DWA system, such as test results from in-house and customer tests of the claimed architecture alone; and customers purchased the DWA system as a direct result of the claimed architecture not advertising or other outside factors.

33. In conclusion, the Examiner would also like to note that, even if the Declaration were sufficient to establish commercial success, the submission of objective evidence of patentability does NOT mandate a conclusion of patentability (MPEP 716.01(d)). In fact, the Examiner believes that the record establishes such a strong case of obviousness that the objective evidence of commercial success alone would not be sufficient to outweigh the evidence of obviousness. In view of the foregoing, when all of the evidence is considered, the totality of the rebuttal evidence of nonobviousness fails to outweigh the evidence of obviousness.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Gottlieb, U.S. Patent Number 6,298,431; Rodgers et al., U.S. Patent Number 6,357,016; and Doing et al., U.S. Patent Number 6,438,671 have taught fine grained multithreading, which interleaves multiple instruction threads for execution in a pipeline.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li
19 January 2007

AJL